SPECIFICATION

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EQUALIZER WITH DECISION FEEDBACK FREQUENCY TRACKING AND BIT DECODING FOR SPREAD SPECTRUM COMMUNICATIONS

Background of Invention

[0001] Field of the Invention. This invention relates to spread spectrum communications systems. More specifically, this invention relates to equalizers with frequency tracking and bit decoding algorithm for spread spectrum communications systems.

[0002] Description of Related Art. A variety of spread spectrum communication system devices and techniques are well known in the art. Typically, in prior systems, significant problems are encountered in spread spectrum receivers where signals from simultaneous transmitters, each with frequency error, must be separated, equalized and decoded.

[0003] Although the following cited U.S. patent documents are not necessarily "prior art," the reader is referred to the following U.S. patent documents for general

background material. Each of these patents is hereby incorporated by references in its entirety for the material contained therein.

[0004] U.S. Patent Nos.: 4,670,885; 4,761,796; 5,168,508; 5,233,626; 5,239,556; 5,596,601; 5,623,511; 5,748,677; 5,825,807; 5,936,997; 6,035,008; 6,047,019; 6,128,329; 6,141,393; 6,175,588; 6,215,762; 6,310,907; 6,473,447; 6,522,683; and 6,556,617.

Summary of Invention

[0005] It is desirable to provide an equalizer and decoder for use in a spread spectrum communication system. Moreover, it desirable to provide an equalizer and decoder for use in a spread spectrum communication system that is capable of handling a continuous stream of data sets from a bank of matched filters with frequency correction.

[0006] Accordingly, it is an object of this invention to provide an equalizer and decoder for use in a spread spectrum communication system that is capable of handling signals from simultaneous transmitters.

[0007] Another object of this invention is to provide an equalizer and decoder for use in a spread spectrum communication system that can separate frequency error associated with transmitters.

[0008] A further object of this invention is to provide an equalizer and decoder for use in a spread spectrum communication system that can equalize frequency error associated with transmitters.

[0009] A still further object of this invention is to provide an equalizer and decoder for use in a spread spectrum communication system that can equalize amplitude error associated with transmitters.

[0010] A still further object of this invention is to provide an equalizer and decoder for use in a spread spectrum communication system that can decode signals from a spread spectrum transmitter.

[0011] Additional objects, advantages, and other novel features of this invention will be set forth in part in the description that follows and in part will become apparent to those of ordinary skill in the art upon examination of the following, or may be learned with the practice of the invention as described herein. The objects and advantages of this invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims. Still other objects of the

present invention will become readily apparent to those skilled in the art from the following description wherein there is shown and described the preferred embodiment of the invention, simply by way of illustration of one of the modes best suited to carry out this invention. As it will be realized, this invention is capable of other different embodiments, and its several details and specific circuits are capable of modification in various aspects without departing from the invention. Accordingly, the objects, drawings and descriptions should be regarded as illustrative in nature and not as restrictive.

Brief Description of Drawings

[0012] The accompanying drawings incorporated in and forming a part of the specification, illustrate present preferred embodiments of the invention. Some, although not all alternative embodiments are described in the following description. In the drawings:

[0013] Figure 1 is a system block diagram showing the major components of one preferred embodiment of the invention.

[0014] Figure 2 is a detailed block diagram of the matched filter architecture of one preferred embodiment of this invention.

[0015] Figure 3 is a set of plots of the IQ signal data.

[0016] Figure 4 is a plot of the PN B matched filter output with no frequency error.

[0017] Figure 5 is a process flow diagram of the basic operations in forming an equalizer block in the method of this invention.

[0018] Figure 6 is a process flow diagram of the packet decode process of the present method of this invention.

[0019] Figure 7 is a set of complex plots of the outputs of the matched filter banks of the present embodiment of this invention.

[0020] Figure 8 is a sequence plot of the 16-bits after the second matched filter of the present embodiment of this invention.

[0021] Figure 9 is a plot of the results of the equalizing and decoding of the present embodiment of this invention.

[0022] Reference will now be made in detail to the present embodiments of the invention, examples of which are illustrated in the accompanying drawings.

Detailed Description

[0023] This invention is spread spectrum communication system that includes an equalizer with decision feedback frequency tracking and bit decoding along with an improved pseudo noise ("PN") code sequencing and matched filter architecture to provide a spread spectrum communication system that is designed to be able to handle a continuous stream of data sets from a bank of matched filters with frequency correction to sort through all the data and successfully decode bits. Processing gain in spread spectrum communications systems can be used to increase the communication channel ("Link") distance and the signal-to-noise ("SNR") margins. Processing gain is itself directly related to the length of the PN code employed. For example, a PN code length of 1000 yields a processing gain of 30 dB, while a PN code length of 10,000 yields a processing gain of 40 dB. In the present invention, long, scalable PN sequences are used with a low-complexity matched filter architecture to provide variable communication rates, robust recovery of multiple devices in ordinary as well as long distance, high interference operating environments. In the present invention sites may receive signals, simultaneously or near simultaneously, from a multitude of transmitting devices. Each of these received signals will typically have a corresponding frequency error. These system requirements tend to preclude locking the receiver to an individual transmitting "client" device in order to achieve frequency coherence across long PN sequences. This invention addresses this problem with a receiver architecture designed

so as to facilitate the "simultaneous" receipt of signals, with a wide range of data rates, from a variety of devices.

[0024] Referring now to figure 1 shows a system block diagram showing the major components of one preferred embodiment of the invention. Data bits 100 are spread 101 by a variable length PNA code 102. Typically, this spread 101 operates to spread the data 100 from 1 to 511 chips, although in alternative embodiments the spread may be varied without departing from the concept of this invention. The resulting chips 106 are further spread 103 by a fixed length PNB code 104. In the present preferred embodiment of the invention, a chipping rate of 5 MCPS is used, further scaling the data rates from 19.608 kbps to 38 bits/second, providing processing gains of from 24 dB to 51 dB, respectively, depending on the application requirements and the available signal-to-noise ratio in the available link (communication channel). The resulting spread data is transmitted, typically using a radio transmitter 105 for use with an RF link. Table 107 shows the performance of a variety of PNA code lengths. As can be seen, with a constant chip rate, here 5 MCPS, as the PNA code length is increased from 1 to 511, the chips per bit increase from 255 to 130305, the processing gain increases from 24 dB to 51 dB and the data rate is reduced from 19608 to 38 bps. Typically, the length of the fixed length PNB code is designed to be short enough to ensure that the worst case frequency error plus the Doppler shift will cause no more than 180 degrees of phase roll, or a correlation loss in the first matched filter of approximately 4 dB.

[0025] Figure 2 shows a detailed block diagram of the matched filter architecture of one preferred embodiment of the method of this invention. The receiver portion of the present data link of this invention includes a radio receiver 201. The output 202 of the receiver 201 provides I & Q channels, which are processed by a matched filter PNB 203 and then by a set of frequency shifters 205, 206, 207, 208, 209, 210, 211, 212. In the present embodiment of the invention, the frequency shifters 205, 206, 207, 208, 209, 210, 211, 212 are arranged forty-five degrees apart. With this architecture the total structure consists of a center frequency (no discernable error) and plus/minus forty-five degree corrections, which in total cover the worst-case frequency error. Because the frequency can be rolling as much as 180 degrees across a single PNB code length, the bank of frequency shifters 205, 206, 207, 208, 209, 210, 211, 212 are used prior to sending the data 204 through the PNA matched filters 213, 214, 215, 216, 217, 218, 219, 220, 221. Although, in this figure 2 eight frequency shifters and nine PNA and one PNB matched filters are shown, the number of each actually employed in a particular embodiment of the invention is dependent on the worst-case frequency roll across the PNB filter. In the present example, approximately 1.3 ppm requires a total of nine banks, including the center frequency filter plus and minus four filters either side of the center frequency. If the total system ppm frequency error is 2.6 ppm, a total of seventeen PNA filters (center bank plus eight frequency shifters on each side) are required. The frequency shifters 205, 206, 207, 208, 209, 210, 211, 212 perform a

complex frequency shift. The PNA matched filters 213, 214, 215, 216, 217, 218, 219, 220, 221 receive data from the frequency shifters 205, 206, 207, 208, 209, 210, 211, 212 and PNB filter 203 and provide a filtered output signals to the equalizer decoder bank 222. The PNB matched filters 203 of the present example of the invention is length 511. While the data output from the first matched filter 203 may still have significant frequency error, the output data from the optimum PNA filter should be within forty-five degrees where the optimum filter is defined as the one with the smallest error. The other filter outputs are typically discardable. But, since there is no practical way to determine which filter is the most correct, data from all filter banks 213, 214, 215, 216, 217, 218, 219, 220, 221 are processed by the equalizer/decoder banks 222 to determine the optimum filter output. In alternative embodiments, the PNA matched filters can be set to other lengths for scalable bit rates. The outputs of the bank of matched filters (PNA) 213, 214, 215, 216, 217, 218, 219, 220, 221 are received by the equalizer / decoder banks 222. The equalizer/decoder banks 222 examines the outputs of each matched filter 213, 214, 215, 216, 217, 218, 219, 220, 221 and determines the frequency shift of the received signal and appropriately selects the set of most advantageous signals.

[0026] Figure 3 shows a set of plots of the IQ signal data. Signals arriving at the equalizer / decoder banks 222 may have originated from multiple transmitters, both near and far, each with frequency errors and unknown bit timing. Furthermore, the I&Q

data coming out of the PNA filters 213, 214, 215, 216, 217, 218, 219, 220, 221 will, in the present example of the invention, typically remain at a sample rate of 40 MSPS and, in alternative embodiments, can be even higher where closer triangulation accuracy is required. Figures 301, 302 shows the I&Q signals respectively coming out of the matched filter bank (PNA) 213, 214, 215, 216, 217, 218, 219, 220, 221. The sum of I and Q is shown in figure 303. The magnitude plot, normalized to 0 dB and plotted as 20*log10 in figure 304. In these plots 301, 302, 303, 304 the data shown represent an ideal case with no frequency error.

[0027] Figure 4 shows a plot 401 of the PN B matched filter output with no frequency error. This plot 401 is a close-up view of the time domain output of the magnitude of a typical PNA matched filter bank 213, 214, 215, 216, 217, 218, 219, 220, 221, with no frequency error shown for clarity. The peaks shown about 0 dB are the correlations at the data rate and occur every 15 PNB lengths, in the present example of the invention. The correlation peaks from approximately -5 to -23 dB are partial correlation products that are due to the use of the concatenated codes. In the present example of the invention, these occur at every PNB chip. The remaining correlations shown from approximately -30 dB, -35 dB and -45 dB and are the cross-correlation products due to the use of binary phase shift keying ("BPSK") modulation of the PN sequences. Because, in the present example of the embodiment of the invention, high chipping and sample rates are used, the matched filters are preferably implemented in

hardware. The present preferred embodiment of invention implements the equalizer and decoder in high-speed DSP chips, although in alternative embodiments, a full hardware, full software, firmware and/or combination of hardware, software and firmware could be used to implement the equalizer and decoder functions, depending on economic conditions and advances in electronics technology. In the present DSP implementation, every sample is not necessarily processed, so long as correlations that are likely to represent bits are processed. In the present example, a PNA of length 15 and a PNB of length 511 are used. A threshold setting of -45 dB below the maximum correlation peaks ensures the reception of distant transmitters and results in processing about 25% of the samples. Therefore, the equalizer block 222 is set to a threshold such that 25% of the samples are forwarded to the decoder block 222. Figure 5 shows the basic operations of the present equalizer 222.

[0028] Figure 5 shows a process flow diagram of the basic operations in forming an equalizer block in the method of this invention. The magnitude of I+Q sample pairs from a single PNA matched filter N are determined 501. If 503, this number is greater than the desired threshold, then the samples are inserted 502 into a queue N along with a time stamp for triangulation. The desired threshold is set by calculating 504 the absolute maximum value of 20 * log 10 (abs (I & Q Samples)) and the running mean and running maximum value is calculated. The desired threshold is set to ensure the reception of distant transmitters and minimize the number of false triggers. In the

present example embodiment, the threshold is set at -45 dB below the peaks and nine input queues are used, where either hardware or a DSP running software tasks can process the samples in the input queues. The queues presently contain periodic time-stamp information such that location based services are provided, in the preferred embodiment, following a successful decode of a message.

[0029] A device, in the present embodiment, sends a packet consisting of a preamble, packet length, device ID, data and CRC, and may include additional data or fields. Knowing the preamble sequence, length and CRC, permits the use of the process further detailed in figure 6 below.

[0030] Figure 6 shows a process flow diagram of the packet decode process of the present method of this invention. For each input queue sample entry 601 the following steps are performed. Assume 602 that this sample is the first bit of a device packet. Create 603 an equalizer using the a-priori known preamble sequence and assume that this equalizer is good. The equalizer is used to decode 604 the packet length. If 605 the decoded packet length is greater than the maximum packet length then stop, otherwise continue. For 1 to packet length equalize/decode 606 the remaining bits. If 607 the CRC is invalid then stop. Otherwise, if 608 the CRC is valid continue. A good packet is received 609. The good packet is passed 610 to the next protocol layer. Input queues are cleared 611 for each sample used. The input queue entries in the remaining frequency bins are cleared 612. This process results in the production of either a

known good packet, because of the CRC check, or it will fail. Because the samples in other frequency bins are identical other than the frequency correction, their queue entries are deleted by the first successful packet decode, thereby avoiding extra computations.

[0031] Figure 7 shows a set of complex plots of the outputs of the matched filter banks of the present embodiment of this invention. The equalization and decoding of bits is presently performed with a signal having a frequency error of -60 degrees per PNB sequence. The figures 701, 702, 703, 704, 705 are complex plots of the outputs of the matched filter banks from -90 degrees to +90 degrees. Figure 701 is a plot of the output at -90 degrees. Figure 702 is a plot of the output at -45 degrees. Figure 703 is a plot of the output at 0 degrees. Figure 704 is a plot of the output at +45 degrees. Figure 705 is a plot of the output at +90 degrees. It can be seen that the output of the -45 degree matched filter, for the example data, is the closest, and it will be used to explain the equalizer / decoder method, since for this example, it is the only one which will result in a successful packet decode. However, as noted above, in the present and alternative embodiments, each output may be processed by the equalizer / decoder. In the case of a single transmitting device, the closest match is the one with the largest peak-to-mean average. In practice with near/far transmitters, it may not always be possible to predict the best bin to start with. In the present example, the PNA sequence

is within 15 degrees of being correct after the frequency correction operation (60 – 45 = 15). Significant frequency roll remains through the PNB sequence.

[0032] Figure 8 shows a sequence plot 801 of the 16-bits after the PNA matched filter of the present embodiment of this invention. Starting at the first peak (assuming it is the correct starting point) the bits are plotted in sequence to illustrate the frequency roll. The equalizer is created for the first bit. It is assumed that it is the first bit of the preamble and it is assumed that the first bit is a digital "one", in which case the actual position after equalization is 1 + 1i. The first equalization ("EQ") position is described in complex vector form as:

[0033] CorrPoint = 1 + i

[0034] EQ = data(1)/EQ

[0035] Eqdata – data(1. . k)/EQ

[0036] where the CorrPoint is the known complex position for a bit equal to one, where the EQ is the complex equalizer formed by a division of the actual first data point (data(1)) and where EQdata is the resulting equalized data set of the first k points.

[0037] The result is a complex vector containing a data set that has been scaled relative to 1 + 1i and has been rotated so that the first point sits at forty-five degrees (1

+ 1i), the correct position of a BPSK modulated "one" bit. The remaining bits are still rotating due to remaining frequency error. The next step is to make an estimate of the frequency roll per bit. This step is accomplished by taking the equalized data points for the length of the preamble and calculating the angles, the delta angles of the preamble and taking a mean value. The result is a (noisy) estimate of the phase roll through the preamble.

[0038] Pream_angle = angle(EQdata(1 . . k)) * 180/π angle - arctan (y/x)

[0039] delta_angles = Pream_angle(k) - Pream_angle(k + 1)

[0040] ang_est = mean(delta_angles)

[0041] where Pream_angle is the resulting angles, k is the length of preamble, angle is computed as arctan(y/x), delta_angles are the differences from point to point and where ang_est is the resulting mean value of the deltas.

[0042] Once the estimate of the phase roll per bit, decoding bits begins. The present process for decoding is as follows:

[0043] (1) The equalizer update rate is set, presently alpha is set to 0.1 and outbits is set to 0.

[0044] (2) The angle of the first sample is set to 45 degrees.

[0045] (3) The first bit of a preamble is presently always set to "one" and the error of the first bit is set to "zero".

[0046] (4) The initial angle is set for the second sample, presently the angles(k) are set according to angles(k) = mod((angle(EQdata(k))*180/pi) + ((k-1) * ang_est), 360).

[0047] (5) The current x-y coordinates of the compensation angle are set, presently y = sin(angle_upd * pi/180) and x = cos(angle_upd * pi/180).

[0048] (6) The complex equalizer value is set Eqxy = x + i*y.

[0049] (7) The error is subtracted, presently if k > 1, EQxy = ((1-alpha)*EQxy) + (alpha * error(k-1)).

[0050] (8) The current vector value is multiplied by EQ rotation, presently outEQdata(k) = (EQdata(k) * EQxy).

[0051] (9) The resulting angle is calculated, presently theta = angle(outEQdata(k)) * 180/pi.

[0052] (10) The decision boundary is computed, presently, if theta > -45 and theta < 135, then outbits(k) = 1.

[0053] (11) The error vector is computed for 1, presently error(k) - (-1+1i) - outEQdata(k).

[0054] (12) The error vector for 0 is computed, presently error(k) = (1+1i) - outEQdata(k).

[0055] (13) The rolling EQ rotation is updated, presently, angle_upd = angle_upd + ang_est.

[0056] The equalization process begins with decision feedback update rate (alpha) and an empty output vector is initialized. A "FOR" loop runs from the send bit to the length of the packet. The angle_upd parameter is used for form a complex EQxy point, which is then multiplied against the data using the alpha factor plus the error term. The complex equalize point is then used to multiply against the next input point to scale and rotate it into position. The decoder forms a decision boundary to decode the bits, and the output bit is generated along with an error vector normalized to the origin. The angle_upd parameter is then updated for the next bit.

[0057] Figure 9 shows a plot 901 of the results of the equalizing and decoding of the present embodiment of this invention. The original bits are shown rolling in frequency. The computed error vector points per bit are shown along with the bits. As can be seen in this plot 901, the equalization/decoding process has removed the error and frequency roll. The described present embodiment of this invention corrects frequency error, while alternative embodiments, for example, can include a full complex equalizer.

[0058] The described embodiment of this invention is to be considered in all respects only as illustrative and not as restrictive. Although specific steps and associated formulas are provided, the invention is not limited thereto. The scope of this invention is, therefore, indicated by the claims rather than by the foregoing description. All changes, which come within the meaning and range of equivalency of the claims, are to be embraced within their scope.